Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 1-7 and 10-18 are pending in the application, with claims 1, 7 and 13 being the independent claims. Claims 8 and 9 are sought to be cancelled without prejudice to or disclaimer of the subject matter therein. Claims 1-7 and 10-18 are sought to be amended. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Objections to the Drawings

The Examiner has objected to FIG. 2 because it is not designated by a legend such as "Prior Art." Accordingly, Applicants have submitted herewith a Replacement Sheet showing FIG. 2, which is designated by a legend "Prior Art." Thus, Applicants respectfully request that the objections to the drawings be reconsidered and withdrawn.

Rejections under 35 U.S.C. § 102

The Examiner has rejected claims 1-18 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,765,771 B2 to Ker *et al.* ("Ker"). Based on the following remarks, Applicants respectfully traverse.

Independent claim 1 is directed to an ESD protection circuit. Claim 1, as amended, includes:

> one or more first diodes on a first area of P-substrate coupled in series between a supply voltage and a terminal pad;
>
> a second diode on said first area of P-substrate coupled to a ground, said second diode having an n+ region; and
>
> one or more third diodes on a second area of P-substrate coupled in series between said terminal pad and said second diode, each of said one or more third diodes having a deep N-well that separates said second area of P-substrate from said first area of P-substrate.

Ker does not teach or suggest the combination of the foregoing features of independent claim 1. For example, Ker does not teach or suggest a second diode on a first area of P-substrate coupled to a ground, the second diode having an n+ region; and one or more third diodes on a second area of P-substrate coupled in series between a terminal pad and the second diode, each of the one or more third diodes having a deep N-well that separates the second area of P-substrate from the first area of P-substrate, as recited in claim 1.

The specification of the instant application provides that the diode structures described therein enable stacking multiple diodes in series on a common IC substrate coupled to ground, while maintaining voltages different form ground at interconnection nodes between the diodes coupled in series between the terminal pad and a diode coupled to ground. (Specification, at paragraph 23).

While Ker appears to describe a silicon controlled rectifier (SCR) structure for stacking SCRs in series (Ker at col. 2, lines 14-15), nowhere does Ker teach or suggest a stack of series diodes that includes a second diode, having an n+ region on a first area of P-substrate, coupled to a ground. Nor does Ker teach or suggest a stack of series diodes that includes one or more third diodes, each having a deep N-well that separates a second area of P-substrate from the first area of P-substrate, coupled in series between a terminal

pad and the second diode. Moreover, the Examiner conceded on page 3 of the Office Action that Ker "does not specifically teach diodes 'D' in deep N wells." Thus, Ker fails to teach or suggest all of the features of independent claim 1, as amended.

Similarly, independent claim 7, as amended, includes:

> one or more first diodes on a first area of P-substrate coupled in series between a supply voltage and a terminal pad, each of said one or more first diodes having a p+ region in an N-well;
>
> a second diode on said first area of P-substrate coupled to a ground, said second diode having an n+ region; and
>
> one or more third diodes on a second area of P-substrate coupled in series between said terminal pad and said second diode, each of said one or more third diodes having an n+ region on said second area of P-substrate separated by a deep N-well from said first area of P-substrate.

For at least the same reasons described above with respect to claim 1, Ker does not teach or suggest each of the features of independent claim 7, as amended. For example, Ker does not anywhere teach or suggest a second diode on a first area of P-substrate coupled to a ground, the second diode having an n+ region; and one or more third diodes on a second area of P-substrate coupled in series between a terminal pad and the second diode, each of the one or more third diodes having an n+ region on the second area of P-substrate separated by a deep N-well from the first area of P-substrate, as recited in claim 7. Thus, Ker fails to teach or suggest all of the features of independent claim 7, as amended.

Likewise, independent claim 13, as amended, includes:

> a first diode on a first area of P-substrate having a cathode coupled to a supply voltage and an anode coupled to a cathode of a second diode, said second diode on said first area of P-substrate having an anode coupled to a terminal pad; and
>
> a third diode on a second area of P-substrate having a cathode coupled to said terminal pad and an anode coupled to a cathode of a

> fourth diode, said fourth diode on said first area of P-substrate having an anode coupled to a ground, wherein said third diode includes an n+ region on said second area of P-substrate separated by a deep N-well from said first area of P-substrate, and wherein said fourth diode includes an n+ region on said first area of P-substrate.

For at least the same reasons described above with respect to claim 1, Ker does not teach or suggest each of the features of independent claim 13, as amended. For example, Ker does not anywhere teach or suggest a third diode on a second area of P-substrate having a cathode coupled to a terminal pad and an anode coupled to a cathode of a fourth diode, the third diode including an n+ region on the second area of P-substrate separated by a deep N-well from a first area of P-substrate; and the fourth diode on the first area of P-substrate having an anode coupled to a ground, the fourth diode including an n+ region on the first area of P-substrate, as recited in claim 13. Thus, Ker fails to teach or suggest all of the features of independent claim 13, as amended.

Since Ker fails to teach or suggest each and every feature of independent claims 1, 7 and 13, as amended, Ker fails to anticipate claims 1, 7 and 13. Furthermore, Ker fails to anticipate claims 2-6, 10-12 and 14-18 for at least the same reasons as independent claims 1, 7 and 13 from which they depend, and further in view of their own features. Claims 8 and 9 are sought to be canceled, and thus, the rejection of those claims under 35 U.S.C. § 102(b) is rendered moot. Accordingly, the Examiner's rejection of claims 1-18 under 35 U.S.C. § 102(b) as being anticipated by Ker is traversed and Applicants respectfully request that the rejection be reconsidered and withdrawn.

The Examiner has rejected claims 1-18 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,616,943 to Nguyen *et al.* ("Nguyen"). Based on the following remarks, Applicants respectfully traverse.

Independent claim 1, as amended, includes:

> one or more first diodes on a first area of P-substrate coupled in series between a supply voltage and a terminal pad;
>
> a second diode on said first area of P-substrate coupled to a ground, said second diode having an n+ region; and
>
> one or more third diodes on a second area of P-substrate coupled in series between said terminal pad and said second diode, each of said one or more third diodes having a deep N-well that separates said second area of P-substrate from said first area of P-substrate.

Nguyen does not teach or suggest the combination of the foregoing features of independent claim 1. For example, Nguyen does not teach or suggest a second diode on a first area of P-substrate coupled to a ground, the second diode having an n+ region; and one or more third diodes on a second area of P-substrate coupled in series between a terminal pad and the second diode, each of the one or more third diodes having a deep N-well that separates the second area of P-substrate from the first area of P-substrate, as recited in claim 1.

Rather, in FIG. 3B, Nguyen appears to show a diode assembly 28, each half of which includes at least three series-connected diodes 34. (Nguyen at col. 4, lines 39-42). FIG. 3A appears to show the structure of the three series-connected diodes 34, each having a p+ active anode 36 and an N-well cathode 38. (Nguyen at col. 4, lines 43-45). Thus, each of the series-connected diodes 34 in assembly 28 has the same diode structure. Nowhere does Nguyen describe connecting in series different diode structures, in particular, a diode structure with an n+ region on a first area of P-substrate and one or

more diode structures with a *deep* N-well that separates a second area of P-substrate from the first area of P-substrate. Accordingly, Nguyen fails to teach or suggest all of the features of independent claim 1, as amended.

For at least the same reasons described above with respect to claim 1, Nguyen does not teach or suggest each of the features of independent claim 7, as amended. For example, Nguyen does not teach or suggest connecting in series diodes having different diode structures. In particular, Nguyen does not teach or suggest one or more first diodes on a first area of P-substrate, each of the one or more first diodes having a p+ region in an N-well, a second diode on the first area of P-substrate, the second diode having an n+ region, and one or more third diodes on a second area of P-substrate, each of the one or more third diodes having an n+ region on the second area of P-substrate separated by a deep N-well from the first area of P-substrate, as recited in claim 7. Thus, Nguyen fails to teach or suggest all of the features of independent claim 7, as amended.

Similarly, for at least the same reasons described above with respect to claim 1, Nguyen does not teach or suggest each of the features of independent claim 13, as amended. For example, Nguyen does not teach or suggest connecting in series diodes having different diode structures. In particular, Nguyen does not teach or suggest a first diode on a first area of P-substrate, a second diode on the first area of P-substrate, a third diode on a second area of P-substrate having an n+ region on the second area of P-substrate separated by a deep N-well from the first area of P-substrate, and a fourth diode on the first area of P-substrate having an n+ region on the first area of P-substrate. Thus, Nguyen fails to teach or suggest all of the features of independent claim 13, as amended.

Since Nguyen fails to teach or suggest each and every feature of independent claims 1, 7 and 13, as amended, Nguyen fails to anticipate claims 1, 7 and 13. Furthermore, Nguyen fails to anticipate claims 2-6, 10-12 and 14-18 for at least the same reasons as independent claims 1, 7 and 13 from which they depend, and further in view of their own features. Claims 8 and 9 are sought to be canceled, and thus, the rejection of those claims under 35 U.S.C. § 102(b) is rendered moot. Accordingly, the Examiner's rejection of claims 1-18 under 35 U.S.C. § 102(b) as being anticipated by Nguyen is traversed and Applicants respectfully request that the rejection be reconsidered and withdrawn.

Rejections under 35 U.S.C. § 103

The Examiner has rejected claims 1-18 under 35 U.S.C. § 103(a) as being unpatentable over Ker in view of Nguyen. Based on the following remarks, Applicants respectfully traverse.

As described above, Ker does not teach or suggest all of the features of independent claim 1, as amended. Furthermore, Nguyen does not supply the missing teachings. At a minimum, any combination of Ker and Nguyen fails to teach or suggest, a second diode on a first area of P-substrate coupled to a ground, the second diode having an n+ region; and one or more third diodes on a second area of P-substrate coupled in series between a terminal pad and the second diode, each of the one or more third diodes having a deep N-well that separates the second area of P-substrate from the first area of P-substrate, as recited in claim 1.

Likewise, as described above, Ker does not teach or suggest all of the features of independent claim 7, as amended, and Nguyen does not supply the missing teachings. At a minimum, any combination of Ker and Nguyen fails to teach or suggest a second diode on a first area of P-substrate coupled to a ground, the second diode having an n+ region; and one or more third diodes on a second area of P-substrate coupled in series between a terminal pad and the second diode, each of the one or more third diodes having an n+ region on the second area of P-substrate separated by a deep N-well from the first area of P-substrate, as recited in claim 7.

Similarly, as described above, Ker does not teach or suggest all of the features of independent claim 13, as amended, and Nguyen does not supply the missing teachings. At a minimum, any combination of Ker and Nguyen fails to teach or suggest a third diode on a second area of P-substrate having a cathode coupled to a terminal pad and an anode coupled to a cathode of a fourth diode, the third diode including an n+ region on the second area of P-substrate separated by a deep N-well from a first area of P-substrate; and the fourth diode on the first area of P-substrate having an anode coupled to a ground, the fourth diode including an n+ region on the first area of P-substrate.

Since neither Ker nor Nguyen, alone or in combination, teaches or suggests all of the features of claims 1, 7 and 13, the combination of Ker nor Nguyen, fails to support a prima facie case of obviousness rejection of claims 2-6, 10-12 and 14-18 for at least the same reasons as independent claims 1, 7 and 13 from which they depend, and further in view of their own features. Claims 8 and 9 are sought to be canceled, and thus, the rejection of those claims under 35 U.S.C. § 103(a) is rendered moot. Accordingly, the

Examiner's rejection of claims 1-18 under 35 U.S.C. § 103(a) is traversed and Applicants respectfully request that the rejection be reconsidered and withdrawn.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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